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Indian Standard

SEMICONDUCTOR DEVICES — INTEGRATED CIRCUITS — SECTIONAL SPECIFICATION FOR FILM INTEGRATED CIRCUITS AND HYBRID FILM INTEGRATED CIRCUITS ON THE BASIS OF THE CAPABILITY APPROVAL PROCEDURES

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Semiconductor Devices and Integrated Circuits Sectional Committee, LT 10

NATIONAL FOREWORD

This Indian Standard, which is identical with IEC Pub 748-22/QC 760200 (1992) 'Semiconductor devices — Integrated circuits — Part 22 : Sectional specification for film integrated circuits and hybrid film integrated circuits on the basis of the capability approval procedures', issued by the International Electrotechnical Commission (IEC). was adopted by Bureau of Indian Standards on the recommendation of Semiconductor Devices and Integrated Circuits Sectional Committee (LT 10) and approval of the Electronics and Telecommunication Division Council.

The text of the IEC standard has been approved as suitable for publication as Indian Standard without deviations. Certain conventions are, however, not identical to those used in Indian Standards. Attention is particularly drawn to the following :

a) Wherever the words 'International Standard' appear referring to this standard, they should be read as 'Indian Standard'.

b) Comma (,) has been used as a decimal marker while in Indian Standards, the current practice is to use a point (.) as the decimal marker.

In the adopted standard, reference appears to certain International Standards for which Indian Standards also exist. The corresponding Indian Standards which are to be substituted in their place are listed below along with their degree of equivalence for the editions indicated :

International Standard	*Corresponding Indian Standard*	*Degree of Equivalence*
IEC Pub 748-20/QC 760000 (1988) Semiconductor devices — Integrated circuits — Part 10 : Generic specification for film integrated circuits and hybrid film integrated circuits	IS QC 760000 (1994) Semiconductor devices — Integrated circuits : Generic specification for film integrated circuits and hybrid film integrated circuits	Identical
IEC Pub 748-21/QC 760100 (1991) Semiconductor devices — Integrated circuits — Part 21 : Sectional specification for film integrated circuits and hybrid film integrated circuits	IS QC 760100 (1995) Semiconductor devices — Integrated circuits : Sectional specification for film integrated circuits and hybrid film integrated circuits	Identical
IEC Pub 748-22-1/QC 760201 (1991) Semiconductor devices — Integrated circuits : Blank detail specification for film integrated circuits and hybrid film integrated circuits on the basis of the capability approval procedures (section 1)	IS QC 760201 (1995) Semiconductor devices — Integrated circuits : Blank detail specification for film integrated circuits and hybrid film integrated circuits on the basis of the capability approval procedures (section 1)	Identical

The concerned technical committee has reviewed the provisions of the IEC Pub 63 (1963), Amendment 1 (1967), Amendment 2 (1977), IEC 68-1, IEC 68-2, IEC 410 (1973) and IEC 747-1 (1983), referred in this adopted standard and has decided that they are acceptable for use in conjunction with this standard.

This standard is intended primarily for use under the IECQ System. A regular Indian Standard for this component could be different, identical or similar to this standard.

Only the English language text in the International Standard has been retained while adopting it in this Indian Standard.

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Indian Standard

SEMICONDUCTOR DEVICES — INTEGRATED CIRCUITS — SECTIONAL SPECIFICATION FOR FILM INTEGRATED CIRCUITS AND HYBRID FILM INTEGRATED CIRCUITS ON THE BASIS OF THE CAPABILITY APPROVAL PROCEDURES

1 Scope and object

1.1 *Scope*

This sectional specification applies to film integrated circuits and hybrid film integrated circuits manufactured as catalogue circuits or as custom-built circuits whose quality is assessed on the basis of the capability approval procedures.

1.2 *Object*

The object of this specification is to present preferred values for ratings and characteristics, to select from the generic specification the appropriate test and measuring methods, and to give general performance requirements to be used in detail specifications for film integrated circuits and hybrid film integrated circuits derived from this specification.

The concept of preferred values is directly applicable to catalogue circuits but does not necessarily apply to custom built circuits.

Test severities and requirements prescribed in detail specifications referring to this sectional specification shall be of equal or higher performance level, since lower performance levels are not permitted.

One or more blank detail specifications, referenced by an IEC number are associated with this specification. When completed as specified in subclause 2.3 of this specification, the blank detail specification forms a detail specification. Such detail specifications shall be used for the granting of capability approval to film integrated circuits and hybrid film integrated circuits according to the boundaries of capability identified by the manufacturer in his capability manual and maintenance of capability approval in accordance with the IEC system.

2 General, preferred characteristics, ratings and severities for environmental, including mechanical tests

2.1 *Related documents*

IEC 748-20/QC 760 000 (1988):	*Semiconductor devices – Integrated circuits – Part 20: Generic specification for film integrated circuits and hybrid film integrated circuits.*
IEC 748-22-1/QC 760 201 (1991):	*Semiconductor devices – Integrated circuits – Blank detail specification for film integrated circuits and hybrid film integrated circuits on the basis of the capability approval procedures (section 1).*

2.2 *Preferred ratings and characteristics*

Preferred values of voltages and currents are given in IEC Publication 747-1; for resistors and capacitors preferred values are given in IEC Publication 63; for custom-built circuits, any values and tolerances may be chosen.

The circuits covered by this specification are classified into climatic categories according to the general rules given in IEC Publication 68-1.

The severities for the cold and dry heat tests are the lower and upper category temperatures respectively. Because of the construction of some circuits, these temperatures will occur between two of the preferred temperatures given in IEC Publication 68-2. In this event, the nearest preferred temperature within the actual range of the circuit shall be chosen for this severity.

2.3 *Information to be given in a detail specification*

Detail specifications shall be derived from the relevant blank detail specification.

Detail specifications shall not specify severities inferior to those of the generic or sectional specification. When more severe requirements are included, they shall be listed in the detail specification and indicated in the test schedules, for example by an asterisk.

NOTE - *The information given on dimensions, characteristics and ratings may, for convenience, be presented in tabular form.*

The following information shall be given in each detail specification and the values quoted shall preferably be selected from those given in the appropriate subclause of this sectional specification.

Each detail specification shall state all the tests and measurements required for lot-by-lot and periodic inspections. This shall, as a minimum, include the relevant tests given in this specification with methods and severities.

Environmental tests (including mechanical), measurements, severities and end-point limits for periodic tests shall be included in the detail specification(s) for the Capability Qualifying Circuits (CQCs). They shall be in accordance with the applicable parts of the generic specification and this specification.

2.3.1 *Outline drawing and dimensions*

There shall be an illustration of the circuit as an aid to easy recognition and for comparison of the circuit with others. Dimensions and their associated tolerances, which affect interchangeability and mounting, shall be given in the detail specification. All dimensions shall be stated in millimetres.

Normally, numerical values shall be given for the length, width and height of the body, and the termination spacing or, for cylindrical types, the body diameter and the length and diameter of the terminations.

When necessary, for example when a detail specification covers more than one package, the dimensions and their associated tolerances shall be placed in a table below the drawing.

When the configuration is other than that described above, the detail specification shall state such dimensional information as will adequately describe the circuit.

2.3.2 *Mounting*

The detail specification shall prescribe the method of mounting to be applied for normal use and for the application of the vibration, bump and shock tests. The design of the circuit may be such that special mounting fixtures are required in its use. In this case, the detail specification shall prescribe the mounting fixtures and they shall be used in the application of the vibration, bump and shock tests.

2.3.3 *Severities for environmental, including mechanical tests*

The detail specification shall prescribe the appropriate method of testing and the appropriate severities selected from section 4 of the generic specification.

2.3.4 *Marking*

The detail specification shall prescribe the content of the marking on the circuit and on the primary package. Deviations from subclause 2.6 of the generic specification shall be specifically stated.

2.3.5 *Ordering information*

The detail specification shall prescribe that the following information is required when ordering circuits:

1) circuit type (e.g. hybrid thick film integrated circuit);
2) number of the detail specification with style reference and assessment level (if appropriate);
3) function of the circuit (if appropriate);
4) basic functional characteristics with tolerance (if appropriate).

2.3.6 *Additional information* (not for inspection purposes)

The detail specification may include information which is not normally required to be verified by the inspection procedure, such as circuit diagrams, curves, drawings and notes needed for clarification.

3 Capability approval procedures

See subclause 3.6 of the generic specification with the following details:

3.1 *Selection of capability qualifying circuits (CQCs)*

3.1.1 The CQCs for approval testing shall be taken from the following sources:

1) special circuits designed to qualify the design rules, processes and products

and/or

2) circuits intended for shipment to customers.

Any or all of these CQCs in combination with process test vehicles shall be adequate to assess the complete design rules, material and manufacturing processes, including any subcontracted process.

Terminations of film elements and added components used for assessment shall be individually accessible for electrical measurement without influence from other circuit elements.

3.1.2 The CQCs shall be used to carry out the tests prescribed for capability approval and for periodic testing, and hence to demonstrate to the NSI that for limiting design layouts:

1) performance limits claimed for individual film element types are achieved;

2) environmental limits claimed for structures intended for shipment are met

and

3) the electrical function performances claimed in the capability manual and the detail specifications are met.

3.1.3 Circuits which have received qualification approval according to IEC Publication 748-21 may be counted as CQCs (provided the requirements of 3.1.1 have been met) for the purpose of capability approval, subject to NSI agreement on relevant structural similarity claims.

3.1.4 A manufacturer who has received capability approval is permitted to obtain a separate qualification approval for any individual circuit he makes, provided all appropriate testing in IEC Publication 748-21 has been completed successfully.

3.1.5 A manufacturer using customer circuits among those selected as CQCs may vary the types tested according to his production plan. In this case the CQCs need not necessarily assess all the claimed limits of his capability all of the time, but they shall be representative of those released during the current maintenance of approval period.

His CQC selection shall be made available to the NSI.

3.1.6 When production material divides into separate processes after a common process, e.g. encapsulation, the common process can be assessed by a single sample.

3.1.7 Where a manufacturer carries out screening tests on all circuits, as a normal production process, he may use screened CQCs for approval.

Where initial screening is not normally carried out or is an option, approval will be carried out on unscreened products.

3.2 *Structural similarity*

1) The CQCs shall be selected by the manufacturer's chief inspector and agreed by the NSI before commencing the approval programme.

2) Rules for structural similarity applicable to the grouping of completed circuits for electrical, dimensional and environmental (including mechanical) tests are given in appendix A of this specification.

3) These rules shall be used to establish the basis of selection for approval. They shall also be used to determine whether new circuits are within the existing approved capability or require its extension to enable their release.

4) Where CQCs are structurally similar for a test sequence, they may be grouped together to form the required numbers in the test tables. Each test sequence has its own structural similarity rules and criteria (see appendix A).

3.3 *Capability approval*

3.3.1 The procedures for capability approval are given in 3.6 of the generic specification.

The test tables for capability approval by CQCs and quality conformance inspection (lot-by-lot and periodic tests) collectively prescribe the minimum test programme on completed circuits.

The manufacturer may select which assessment level K, L or M he wishes to include, but a manufacturer with approved capability may only release products as follows:

Assessment level	*Release assessment levels*
K	K, L or M
L	L or M
M	M

NOTE - The suffix "N" is used if necessary to denote nonqualified components. See generic specification, subclause 3.6.2.3.

A manufacturer may upgrade the assessment level of his approval by following the procedures given in the generic specification and he may downgrade without further periodic testing until current test interval dates expire. In either case the NSI shall be notified.

Any additional test required for specific applications shall be given in the detail specification and be subject to agreement between the customer and manufacturer.

The post-test electrical limits for the relevant environmental tests shall be given in the detail specification.

3.3.2 *Release for delivery before completion of group B tests*

Due to the need for extended periods of lot collection from small quantity production batches, a manufacturer may, with the agreement of the customer, release products in advance of group B tests provided that the previous lot of identical circuits passed satisfactorily.

In this case, he shall indicate clearly on the relevant release documents that the circuits are released under subclause 3.3.2 of this specification and complete the tests within one month of despatch.

In the event of subsequent failure to meet environmental tests, all products which have been released in advance may be subject to recall or quarantine, dependent on the reason for failure.

3.3.3 *Capability approval (fixed sample size procedures)*

3.3.3.1 *Sampling*

The sample size and criteria of acceptability depend on the assessment level which is claimed and are detailed in table 2.

When additional groups are introduced into the test schedule, the number of circuits required for group "0" shall be increased by the same number as that required for the additional groups.

3.3.3.2 *Tests*

The tests in table 1 are intended to validate the design rules, materials, processes, piece parts and package range by testing all the CQCs and process test vehicles.

For each test group, different CQCs may be grouped together according to the structural similarity rules given in appendix A, to reach the required number of samples for that group.

The complete series of tests specified in table 1 is required for the approval of capability covered by the capability manual. The tests in each group shall be carried out in the given order.

The required portions of the sample shall be subjected to the tests of group "0" and then the total sample divided for the other groups.

Circuits found defective during the tests of group "0" shall not be used for the other groups.

"One defective" is counted when a CQC has not satisfied the whole or part of the tests of a group.

The approval is granted when the number of defectives does not exceed the specified number of permissible defectives for each group or sub-group and the total number of permissible defectives.

Table 1 - Test schedule for qualification approval

Sample sizes and acceptance criteria are detailed for each assessment level in table 2.

Subclause numbers refer to section 4 of the generic specification.

Subclause numbers, tests and test sequences	D or ND	Test conditions	Performance requirements
Group 0 *Sub-group 01* 4.3.1 Precap visual examination	ND		
Sub-group 02a 4.3.2 External visual and marking examination	ND		
Sub-group 02b 4.3.3 Dimensions			
Sub-group 03 (Note 7) 4.5.16 Induced flammability (for information only)	D		
Sub-group 04 (Note 1) 4.5.9 Sealing	ND		
Sub-group 05 4.4.11 Major static and dynamic electrical characteristics at room temperature	ND		
Sub-group 06 4.4.11 Major static and dynamic electrical characteristics at extreme operating temperatures	ND		
Group 1 Sequence (Notes 1 and 2) Initial measurements 4.5.6 Vibration, swept frequency and 4.5.7 Acceleration, steady state or 4.5.5 Shock and 4.5.7 Acceleration, steady state Final measurements	D/ND	4.4.11: Sub-group 05 4.5.9: Sealing 4.4.11: Sub-group 05	

For notes, see next page.

Table 1 (*continued*)

Subclause numbers, tests and test sequences		D or ND	Test conditions		Performance requirements
Group 2	Sequence	D			
Initial measurements			4.4.11:	Sub-group 05	
4.5.11	Resistance to soldering heat				
4.5.15.2	Resistance to solvents (Note 7)				
4.5.8	Change of temperature				
4.5.3	Damp heat, steady state (Note 4)				
Final measurements			4.5.9: 4.4.11: 4.3.2:	Sealing (Note 1) Sub-group 05 External visual and marking examination	
Group 3	Sequence (Note 5)	D			
4.5.10	Solderability				
4.5.12.1	Tensile				
	Bending (wire or strip)				
Final measurement			4.5.9:	Sealing (Note 1)	
	or (Note 3)				
4.5.10	Solderability				
4.5.12.1	Tensile				
4.5.12.3	Bending (row)				
4.5.12.2	Thrust				
Final measurements			4.5.9:	Sealing (Note 1)	
Group 4	Sequence	ND			
Initial measurements			4.4.11:	Sub-group 05	
4.5.2	Cold		Temperature: ..... °C		
4.5.1	Storage at high temperature		Temperature: ..... °C		
Final measurements			4.4.11:	Sub-group 05	
Group 5		D			
Initial measurements			4.4.11:	Sub-group 05	
4.5.14	Endurance: 1 000 h				
	Endurance: 2 000 h (Note 6)				
Final measurements			4.4.11:	Sub-group 05	

NOTES

1 Cavity circuits only.

2 Mounting conditions as recommended by the detail specification.

3 The detail specification shall state which option is to be used.

4 The detail specification may delete the damp heat test for unencapsulated circuits.

5 Use of completely processed electrical rejects is permitted.

6 In assessment level K: provisional approval after 1 000 h;
definitive approval after 2 000 h.

7 Applicable to encapsulation having organic material used for sealing purposes.

8 Not required for CQCs.

3.3.4 *Maintenance of capability approval*

3.3.4.1 *Screening and lot-by-lot acceptance tests*

The screening and testing on a lot-by-lot basis, for all circuits intended for release to customers are prescribed in the blank detail specification, table 2.

For group A and B tests, the sample shall be collected from one week's production, or such other period as declared by the manufacturer up to a maximum of one month.

3.3.4.2 *Periodic tests*

The periodic tests for CQCs are prescribed in table 3 and the blank detail specification.

Where customer circuits are used as CQCs, samples for periodic testing shall be drawn from lots which have passed the tests of screening when appropriate and lot-by-lot inspection.

Provisional capability approval may be granted after 1 000 h.

3.3.4.3 *Tests*

The complete series of tests specified in the blank detail specification is required for the maintenance of capability approval.

The tests in each group shall be carried out in the order given.

"One defective" is counted when a circuit has not satisfied the whole or a part of the tests of a group.

The approval is maintained when the number of defectives does not exceed the specified number of permissible defectives for each group and the total number of permissible defectives.

3.3.5 *Special requirements*

Small production lots (under consideration).

3.3.6 *Quality conformance inspection*

3.3.6.1 *Test schedule*

The schedule for the lot-by-lot and periodic tests for quality conformance inspection is given in tables 2 and 3 of the blank detail specification.

3.3.6.2 *Assessment levels*

The assessment level(s) for capability approval (see table 1) and for maintenance of capability approval (see relevant blank detail specification) shall be selected from tables 2 and 3 hereafter.

Table 2 - Assessment levels and acceptance criteria for initial capability approval

In this table: *n* = sample size;

c = acceptance criterion (permitted number of defectives).

<table>
<tr><th rowspan="3">Inspection group or sub-group of table 1</th><th colspan="9">Assessment level</th></tr>
<tr><th colspan="3">K</th><th colspan="3">L</th><th colspan="3">M</th></tr>
<tr><th><i>n</i></th><th colspan="2"><i>c</i></th><th><i>n</i></th><th colspan="2"><i>c</i></th><th><i>n</i></th><th colspan="2"><i>c</i></th></tr>
<tr><td>01</td><td>Required</td><td colspan="2">–</td><td>–</td><td colspan="2">–</td><td>–</td><td colspan="2">–</td></tr>
<tr><td>02a</td><td>75 (Note 1)</td><td colspan="2">2</td><td>64 (note 1)</td><td colspan="2">2</td><td>43</td><td colspan="2">2</td></tr>
<tr><td>02b</td><td>8</td><td colspan="2">1</td><td>8</td><td colspan="2">1</td><td>8</td><td colspan="2">1</td></tr>
<tr><td>03 (for information only)</td><td>2</td><td colspan="2">–</td><td>2</td><td colspan="2">–</td><td>2</td><td colspan="2">–</td></tr>
<tr><td>04</td><td>39</td><td>1</td><td rowspan="3">2</td><td>26</td><td>1</td><td rowspan="3">2</td><td>13</td><td>1</td><td rowspan="3">2</td></tr>
<tr><td>05</td><td>71 (Note 1)</td><td>1</td><td>60 (Note 1)</td><td>1</td><td>39</td><td>1</td></tr>
<tr><td>06</td><td>26</td><td>1</td><td>13</td><td>1</td><td>8</td><td>1</td></tr>
<tr><td>1</td><td>10</td><td>1</td><td rowspan="4">2</td><td>8</td><td>1</td><td rowspan="4">2</td><td>–</td><td>–</td><td rowspan="4">2</td></tr>
<tr><td>2 (Note 2)</td><td>13</td><td>1</td><td>10</td><td>1</td><td>8</td><td>1</td></tr>
<tr><td>3</td><td>13</td><td>1</td><td>10</td><td>1</td><td>8</td><td>1</td></tr>
<tr><td>4</td><td>13</td><td>1</td><td>10</td><td>1</td><td>8</td><td>1</td></tr>
<tr><td>5 (1 000 h)</td><td>–</td><td colspan="2">–</td><td>20</td><td colspan="2">1</td><td>13</td><td colspan="2">1</td></tr>
<tr><td>(2 000 h)</td><td>20</td><td colspan="2">1</td><td>–</td><td colspan="2">–</td><td>–</td><td colspan="2">–</td></tr>
</table>

NOTES

1 This number may be reduced by the relevant number of circuits which are not needed when the tests in group 1 are not required.

2 A minimum of four circuits shall be used for each solvent specified.

Table 3 - Assessment levels and acceptance criteria for quality conformance inspection

Table 3A - Lot-by-lot tests to be conducted on a sampling basis

In this table: *IL* = inspection level;

AQL = acceptable quality level.

Subclause numbers refer to section 4 of the generic specification.

Inspection group or sub-group	Assessment level					
	K		L		M	
Screening (see table 4)	Required		Not required		Not required	
	IL	*AQL*	*IL*	*AQL*	*IL*	*AQL*
Sub-group A1 4.3.2 External visual and marking examination	II	1	II	2,5	I	2,5
Sub-group A2 4.4.11 Major static and dynamic electrical characteristics at room temperature	II	0,25	II	0,4	II	1
Sub-group A3 4.4.11 Major static and dynamic electrical characteristics at extreme operating temperatures	S4	1	-	-	-	-
Sub-group B1 4.5.10 Solderability	S3	2,5	S3	2,5	S3	2,5
Sub-group B2 4.3.3 Dimensions	S4	1	S4	1	S4	1

Table 3B - Periodic tests to be conducted on a sampling basis

In this table: *p* = periodicity (in months);
n = sample size;
c = acceptance criterion (permitted number of defectives);
Subclause numbers refer to section 4 of the generic specification.

Inspection group or sub-group	Assessment level											
	K				L				M			
	p	*n*	*c*		*p*	*n*	*c*		*p*	*n*	*c*	
Sub-group C1 4.4.11 Major static and dynamic electrical characteristics at extreme temperatures (Note 8)	–	–	–		6	13	1		6	8	1	
Sub-group C2 Sequence (Notes 1 and 2) 4.5.6 Vibration, swept frequency and 4.5.7 Acceleration, steady state or (Note 3) 4.5.5 Shock and 4.5.7 Acceleration, steady state	6	10	1	2	12	8	1	2	–	–	–	2
Sub-group C3 Sequence 4.5.11 Resistance to soldering heat 4.4.15.2 Resistance to solvents (Note 7) 4.5.8 Change of temperature 4.5.3 Damp heat, steady state (Note 4)	6	13	1		12	10	1		12	8	1	
Sub-group C4 Sequence 4.5.2 Cold 4.5.1 Storage at high temperature	6	13	1		12	10	1		12	8	1	
Sub-group D1 4.5.14 Endurance: 1 000 h	–	–	–		6	20	1		6	13	1	
Endurance: 2 000 h (Note 6)	3	20	1		–	–	–		–	–	–	
Sub-group D2 Sequence (Note 5) 4.5.12.1 Tensile 4.5.12.3 Bending (wire or strip) or (Note 3) 4.5.12.1 Tensile 4.5.12.3 Bending (row) 4.5.12.2 Thrust	12	13	1		12	10	1		12	8	1	
4.5.16 Induced flammability (Note 7) (for information only)	12	2	–		12	2	–		12	2	–	

Notes on page 8, after table 1.

Table 4 – Screening

Sequences for screening shall be in accordance with table 4.

Steps	Examination or test	Generic specification reference	Details and conditions	Sequences				
				A	B	C	D	E
1*	Precap visual inspection	4.3.1	Under consideration	x				
2	Storage at high temperature	4.5.1	24 h at maximum storage temperature	x	x	x		x
3	Change of temperature	4.5.8	10 cycles T_{stg} min. : T_{stg} max.	x	x	x		x
4*	Acceleration, steady state	4.5.7	In the most critical direction. Acceleration level as specified in the detail specification	x	x	x		
5*	Sealing	4.5.9		x	x	x		
6	Electrical measurements (pre burn-in)		Selected parameters Remove defective devices (Note 1)	x	x		x	
7	Burn-in		As specified in the detail specification hours:	x 168	x 72		x 48	
8	Electrical measurements (post screening)		As specified in 6 Remove defective devices Reject lot if defects exceed 10 %	x	x	x	x	x

* Not normally applicable to non-cavity devices, unless specified in the detail specification.

NOTES

1 Record the results of the measurements unless otherwise specified in the detail specification.

2 Screening is normally performed before group A, B and C inspection. When screening is performed after meeting the requirements of groups A and B on a lot-by-lot basis and group C on a periodic basis, the solderability, sealing and group A tests shall be repeated.

Additional post-screening tests may be required as specified in the blank detail specification.

3.4 *Resubmission of rejected lots (lot-by-lot inspection)*

Any lot rejected following electrical tests shall be returned to production for rework or rescreening for the identified defect. No new circuit shall be included in the lot.

The lot shall then be resubmitted and inspected under conditions of tightened inspection.

It will retain the same lot number and details of the new submission will be recorded. The same lot shall not be submitted more than three times.

3.5 *Manufacturing stages in a factory of an approved manufacturer in a non-IEC member country*

The application of the extension of the manufacturer's approval is permitted for the film integrated circuits and hybrid film integrated circuits covered by this sectional specification, provided that the conditions of subclause 3.2 of the generic specification are met.

4 Test and measurement procedures

This clause contains all the tests and measurement procedures which are of typical application for film integrated circuits and hybrid film integrated circuits and which are not described in section 4 of the generic specification.

Each detail specification shall state all the tests and measurement procedures required for lot-by-lot inspection and periodic testing. It shall, as a minimum, include the relevant tests given in this specification with stated methods and severities.

Environmental tests, measurements, severities and end-point limits for periodic tests of the CQCs shall be included in the detail specification. They shall be in accordance with the applicable numbers of the generic specification and this sectional specification.

Appendix A

Structural similarity rules for capability approval

General

This appendix defines the rules for deciding if a new circuit is covered by the manufacturer's declared capability and the testing performed on CQCs. It may also be used as a guide to the manufacturer in selecting CQCs to cover a capability. Where the rules do not cover specific circumstances, the manufacturer's chief inspector and the NSI shall agree upon the additional criteria and shall submit a subsequent proposal for amendment of this document through their national committee.

Structural similarity rules

When structural similarity is to be decided upon, the following procedures shall be considered.

A.1 Defining CQC(s) within the structural similarity rules

i) Table A.10 is structured to align with test sequences given in table 1 of this specification and table 3 of the blank detail specification.

Circuits selected for the periodic inspection schedules shall also be representative of the circuits currently in production.

Having first classified the circuit according to table 1 in the generic specification, the manufacturer should use table A.1 in this specification to classify the materials, processes and basic technology which represent his capability.

ii) The manufacturer should then review his current and/or intended range of products against the similarity combination rules given in tables A.2 to A.7 and A.10. This enables a decision to be made on the number of different CQC types needed for capability approval from the technological standpoint.

iii) The selection process then extends to tables A.8 and A.9 which define the limits of combination for mass and dimensions.

Additional CQCs to those nominated in ii) above may be required to cover these aspects.

iv) After choosing suitable environmental test severities from section 4 of the generic specification, a chart can be constructed which shows the tests and severities applicable to each CQC.

v) The structural similarity of a circuit with a CQC (or CQCs) requires that the layout design rules used, and electrical and environmental ratings and characteristics shall not be more severe than those for the CQCs.

Generally the choice of CQCs lies between:

- special circuits designed to cover as many capability boundaries as is practicable with each type; this will result in the minimum number of CQC types;

or

- the use of a wider range of normal custom/catalogue circuits as CQCs to cover the capability.

A.2 New circuits

Each new circuit to be manufactured for sale and release within the system shall first be checked to ensure that it can be constructed using validated design rules, contains validated materials and can be made using approved processes and package styles.

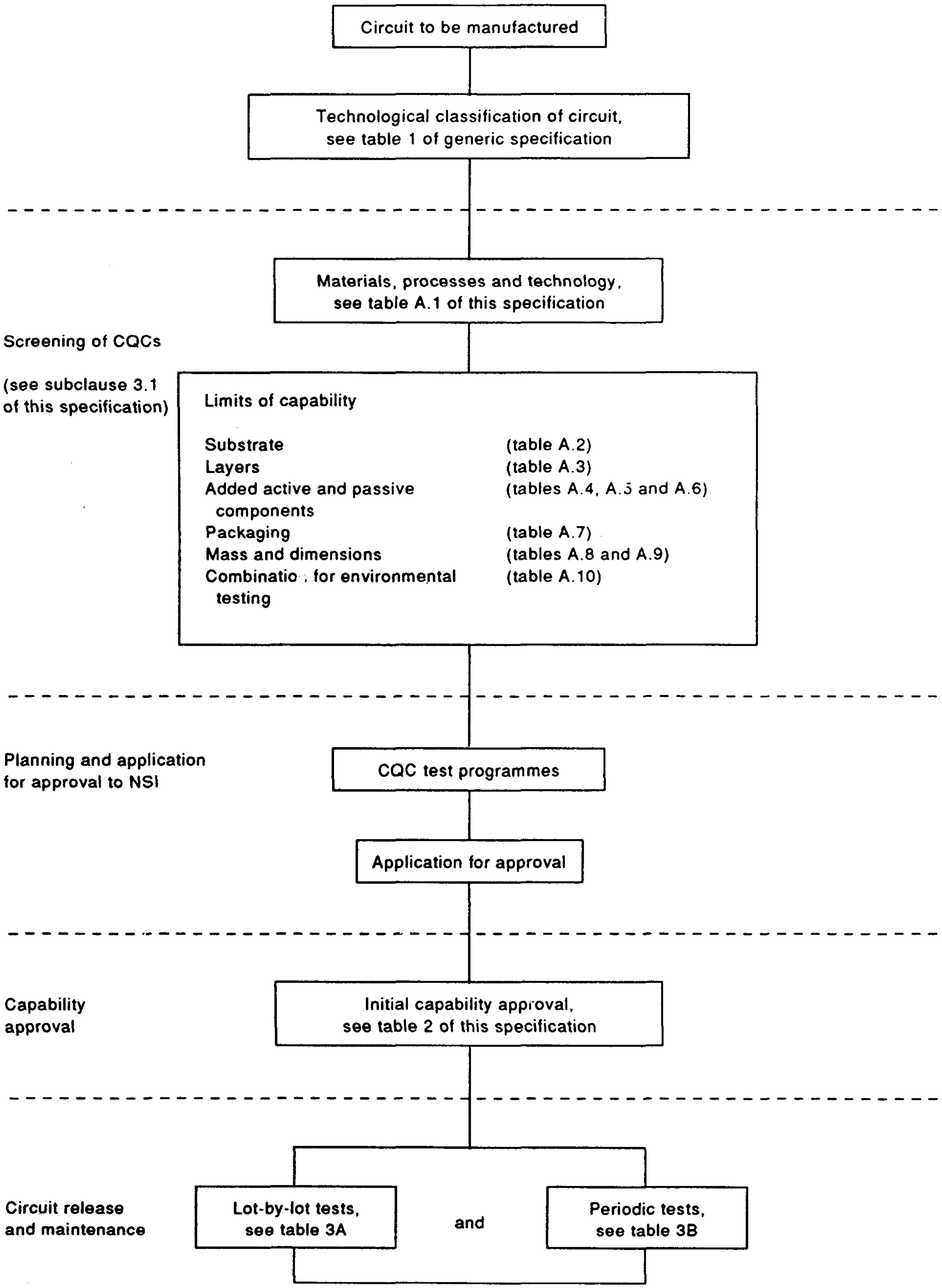
Next, its features should be considered in relation to existing CQCs, i.e. for the cover they give in terms of materials and technology (tables A.2 to A.7), mass and dimensions (tables A.8 and A.9), appropriate tests and severities (table A.10 and section 4 of the generic specification). Its features shall be covered by one or more CQC.

Where existing CQCs do not cover the new circuit, the manufacturer wishing to release it shall first extend his capability in accordance with the specific need and the requirements of subclause 3.6.3.5 of the generic specification. In this case the extra tests may be performed either on a CQC or on the new circuit itself.

A.3 Guidance on procedures

The diagrams below give guidance on the implementation of the principles described in A.1 and A.2 above.

A.3.1 *Screening and testing of CQCs for capability approval*


Circuit to be manufactured
Technological classification of circuit, see table 1 of generic specification
Materials, processes and technology, see table A.1 of this specification
Screening of CQCs
(see subclause 3.1 of this specification)
Limits of capability
Substrate (table A.2)
Layers (table A.3)
Added active and passive components (tables A.4, A.5 and A.6)
Packaging (table A.7)
Mass and dimensions (tables A.8 and A.9)
Combination for environmental testing (table A.10)
Planning and application for approval to NSI
CQC test programmes
Application for approval
Capability approval
Initial capability approval, see table 2 of this specification
Circuit release and maintenance
Lot-by-lot tests, see table 3A
and
Periodic tests, see table 3B

A.3.2 *Procedure for new circuits*

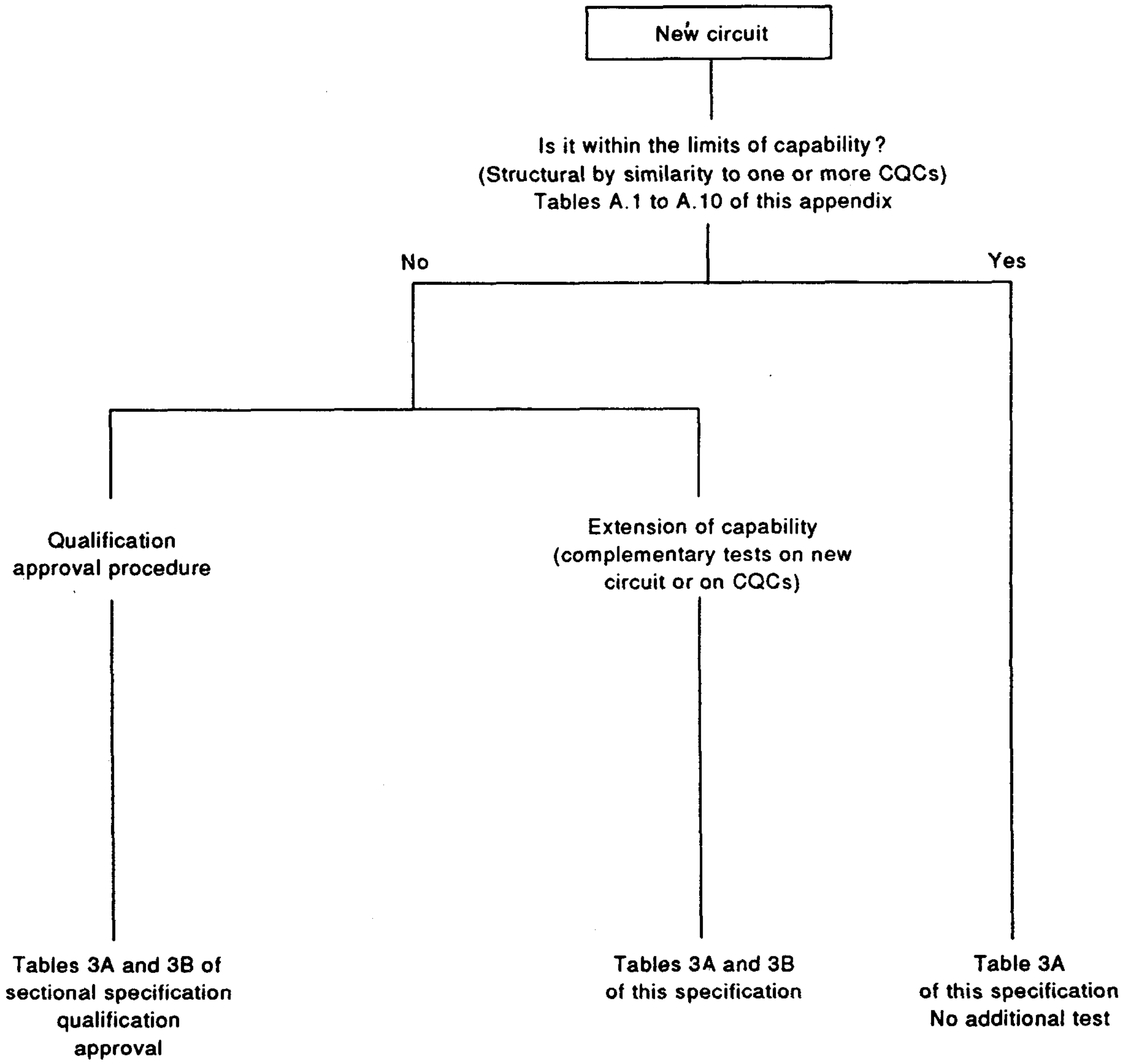

New circuit
Is it within the limits of capability?
(Structural by similarity to one or more CQCs)
Tables A.1 to A.10 of this appendix
No
Yes
Qualification approval procedure
Extension of capability (complementary tests on new circuit or on CQCs)
Tables 3A and 3B of sectional specification qualification approval
Tables 3A and 3B of this specification
Table 3A of this specification No additional test

Table A.1 – Classification of technology, materials and processes

- Individual statements in each of the columns below give examples of materials, processes and technologies to which tables A.2 to A.7 may be applied.
- The list of items is not necessarily complete.
- Items listed in the various columns are not necessarily linked horizontally.

Items	Basic technology	Basic materials	Basic processes/methods
Substrates (Table A.2)		Alumine Glass Coated metal Beryllia Sapphire Quartz Silicon Organic	Pressed/slip-cast Flame polished Lapped and polished
Film elements (Table A.3) a) Function such as: Resistors Capacitors Inductors Thermistors Opto-electronic devices Conductors Crossovers Via holes Active devices		*Thick film:* Loaded organic Copper Ruthenium Gold Palladium-silver Palladium-gold Platinum-silver Platinum-gold Glass-ceramic	*Thick film:* Deposited and fired
		Thin film: Copper Tantalum nitrid/oxide Nickel, chromium, Nickel-chromium Gold Tungsten Titanium Palladium Platinium Molybdenum Molymanganese Magnesium Aluminium Silicon oxide/nitride Organic materials	*Thin film:* Evaporation Sputtering Plating Spinning (centrifugal) Dip lacquering Anodization
b) Pattern generation (mainly thin film)			Metal mask Photolithography Additive Subtractive Laser machine Ion beam Electron beam

Table A.1 *(continued)*

Items	Basic technology	Basic materials	Basic processes/methods
d) Multilayer	Organic dielectric Inorganic dielectric	Conductors and insulators	*Thick film:* Sequential print and fire Laminated, press and cure/fire
			Thin film: Sequential vacuum deposition Spinning (centrifugal) Dip lacquering Anodization Sputtering
Added components (Tables A.4, A.5, A.6)			
Diodes Transistors Integrated circuits	Encapsulated Hermetic Plastic Chip carrier Tape leads Wire leads	Germanium Silicon Ga As P	Eutectic Adhesive Solder preform Solder paste
Opto-electronic Resistors Capacitors Inductors	Non-encapsulated Passivated Non-passivated Face-up Flip chip Beam lead Spider	Thick film Nickel-chromium Tantalum Diffused silicon	Wire-bond A1, Au Thermo-compression Ultrasonic Thermo-pulse Solder reflow Resistance weld Thermosonic
		Ceramic Tantalum Foil Silicon	Adhesive Wire, soldered
Packaging (Table A.7)	Basic style and form: Leadless Dual-in-line Single-in-line Flat-pack Chip carrier Non-encapsulated Hermetic Moulded plastic Conformal coating	Basic encapsulation materials: Metal Ceramic Metal-ceramic Metal-glass Organic Silicone	Method of closure/ encapsulation: Glass/metal seal Organic seal Resistance weld Laser weld Solder seal Electron beam weld Cast mould Injection mould Plastic box fill Dip coat Drop coat Spray coat Fluidized bed

Table A.2 - Substrates

Characteristics	Similarity rules
Material	For combination, the proportion of main material representing at least 90 % of the substrate volume shall be equal to within 2 %
Thickness	Same nominal substrate thickness
Size (*L* = length of CQC) (*l* = width of CQC)	Combinations allowable for: 0,2 L ≤ length ≤ 2 L 0,2 W ≤ width ≤ 2 W
Mechanical parameters: - camber - roughness - porosity - appearance	Same purchase and inspection specifications

Table A.3 – Film materials

Characteristics	Similarity rules
1 – Conductive materials (type, composition)	Same
2 – Basic process	Same
3 – Multilayers (type, dielectric, composition)	Any combination within the maximum number of layers on the CQC
4 – Resistive materials: - composition	Same material series
- resistivity per square	Any combination within the range of extreme values covered by CQC
Maximum power per unit area of resistor elements	Any combination limited to the maximum power rating covered by CQCs
Trimming process	Same trimming process, e.g. laser, airbrasion, spark erosion
Resistance values and tolerance	For a given tolerance, combination allowed within the range of minimum and maximum resistance values covered by the CQCs
Temperature coefficient	Combination allowed within guaranteed absolute values of the CQC
Differential temperature coefficient and differential ohmic value tolerance	Combination allowed in the range of extreme ohmic values of the CQCs
Number of resistive elements	No limitation
Interconnection mode	Same
5 – Protective coatings	Same

Table A.4 – Added non-encapsulated active chip components (note 1)

Characteristics	Similarity rules
Component type (notes 2 and 3)	
1) Transistor and diode 2) Integrated circuit	Combination allowed within 1) or 2) but not between these two generic families
Presentation of components	
1) Diffusion face-up 2) Diffusion face-down	Combination allowed within 1) or 2) but not between these two presentations
Methods of mounting	
Adhesive, eutectic, soldering, other	Combination allowed within but not between these mounting methods
Wiring	
a) Materials (gold wire, aluminium wire, other)	No combination allowed between different basic metal wires
b) Methods (thermocompression, thermosonic, other)	No combination allowed between different bonding methods
c) Wire diameter	Combination allowed within ±50 % of wires used in CQCs
d) Tape cross-sectional area	Combination allowed within ±50 % of sectional area used in CQCs
Dimensions	
1) Semiconductor chip area	Combination allowed within ±50 % of the smallest and 200 % of the largest chip on the CQC
2) Integrated circuit chip area	Combination allowed within ±50 % of the smallest and 200 % of the longest chip on the CQC
3) Number of outputs	Any combination allowed
Protective coatings	Same coating material, chip technology and passivation combination

NOTES

1 When non-qualified added components are given qualified status by the procedures in 3.6.2.2 of the generic specification, structural similarity rules for hybrid circuits require the same manufacturing source for each added component.

2 If the CQC has no integrated circuit, the number of transistors or diodes shall be a minimum of three.

3 If the hybrid CQC contains one or more monolithic circuit chips, the ratio of the total number of wires bonded to the chip(s) to the total number of electrically connected CQC package leads shall be equal to or greater than 0,5.

Table A.5 – Added encapsulated active components other than chips (note 1)

Characteristics	Similarity rules
Component type (notes 2 and 3) 1) Transistor and diode 2) Integrated circuit	Combination allowed within but not between these two generic families
Presentation of component 1) Encapsulated components with leads 2) Encapsulated components without leads	For a given encapsulation style, combination allowed within but not between the presentation categories 1) and 2), and also within 200 % of the number of leads on the encapsulated component on the CQC
Mounting methods and interconnections Soldering, adhesive, welding	Combination allowed within but not between these mounting methods
Component encapsulation	No combination allowed unless: 1) The environmental classification of the component is the same or higher than the environmental classification of the CQC or 2) The CQC is hermetically sealed

NOTES

1 When non-qualified added components are given qualified status by the procedures in 3.6.2.2 of the generic specification, structural similarity rules for hybrid circuits require the same manufacturing source for each added component.

2 If the specimen has no integrated circuit, the number of transistors or diodes shall be a minimum of three.

3 If the hybrid CQC contains one or more monolithic integrated circuits, the ratio to the total number of connected integrated circuit leads to the total number of electrically connected CQC package leads shall be equal to or greater than 0,5.

Table A.6 – Added passive components (note 1)

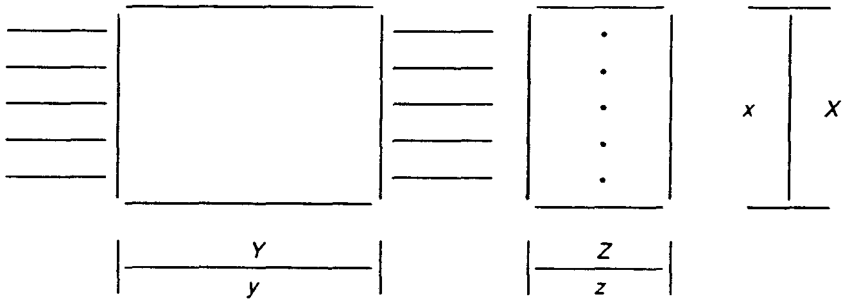
Characteristics	Similarity rules
Component type	
1) Components with leads 2) Components without leads	No combination allowed between 1) and 2) but any combination allowed within each component family covered by CQCs, e.g. ceramic capacitors class I, resistors chips, etc.
Mounting methods and interconnections	
Soldering, adhesive, wire-bonding, welding	Combination allowed within but not between these methods
Dimensions	
Assessment levels K and L	Combination allowed within the limit of double or half the lateral dimensions of each component used in the CQCs
Assessment level M	Any combination allowed

NOTE 1 – When non-qualified added components are given qualified status by the procedures in 3.6.2.2 of the generic specification, structural similarity rules for hybrid circuits require the same manufacturing source for each added component.

Table A.7 – Package

Characteristics	Similarity rules
Encapsulation process	
1 – Non-encapsulated	Combination within the limits of the substrate size (see table A.2) and same lead attachment methods and materials
2 – Embedded 3 – Cavity (inorganic seal)	No combination allowed between different material and protective coating systems
Package material	Same
Sealing material	Same
Filling	Same or lesser humidity content (dew-point)
4 – Cavity (organic seal)	
Package material	Same
Sealing material	Same
Filling	Same or lesser humidity content (dew-point)
Lead	
1 – Material, process and coating	Same material for leads and insulating material
2 – Seal lead length	Same or greater
3 – Material and method of connection to substrate	Same
4 – Mechanical material characteristics	Same or greater
5 – Spacing	Same or greater
6 – Dimensions	Same or greater cross-sectional area
Marking system and method of application	Any possible system and method of application
Substrate attachment	Same material and process

Table A.8 – Mass and dimensions of package



Parameter	CQC or master circuit	Associated devices	Limits (notes 1 and 2)
Length	X	x	$aX \leq x \leq b$
Width	Y	Y	$aY \leq y \leq bY$
Surface	$S = XY$	$s = xy$	$eS \leq s \leq fS$
Thickness	Z	z	$gZ \leq z \leq hZ$
Number of terminations	N	n	$uN \leq n \leq vN$
Mass	M	m	$jM \leq m \leq kM$
Mass per termination	M/N	m/n	$w\ M/N \geq m/n$ (note 3)

NOTES

1 Where there are two limits, the more severe shall be considered.

2 For cylindrical packages, the same rule with $X = Y =$ diameter is applied.

3 This criterion is applicable only where the mechanical tests are carried out with the circuit fixed by its terminals. It is not applicable to cylindrical packages with diameter less than 15,41 mm nor to rectangular packages with dimensions less than 17 mm x 17 mm.

Table A.9 – Limits of association in relation with mass and dimensions

Assessment levels (Notes 1 and 2)	a	b	e	f	g	h	j	k	u	v	w
K	0,2	1,5	0,1	1,5	0,8	1,2	0,2	1,8	0,5	2	1,2
L	0,2	2	0,1	2	0,5	1,5	n.a.	n.a.	0,3	2	n.a.
M	0,2	2	n.a.	n.a.	0,5	1,5	n.a.	n.a.	n.a.	n.a.	n.a.

NOTES

1 "n.a." means "not applicable".

2 The letters used in the headings correspond to those of column 4 of table A.8.

Table A.10 – Combination criteria for environmental, including mechanical, testing

This table serves as the basis for establishing test programmes for the assessment or the extension of a claimed capability. This table aligns with table 1 of this specification and tables 2 and 3 of the blank detail specification.

It specifies per test group the technological aspects and criteria to be met for deciding on structural similarity between a given non-encapsulated or embedded circuit and/or CQCs.

When one or more of the criteria of a test group are not met, structural similarity principles cannot be applied and the manufacturer's capability has to be extended to cover the particular requirements for that test group.

NOTE - Requirements are either mandatory (x) or not applicable (–).

No.	Unencapsulated	Embedded	Cavity (organic seal)	Cavity (inorganic seal)	Criteria	Notes
Applicable test table: – sealing (cavity circuits only) *Sub-group 04*						
1	–	–	X	X	Same or less severe test schedule(s) and/or conditions	
2	–	–	X	X	Same package style/material and construction method (table A.7)	
3	–	–	X	X	Similarity within table A.8	
4	–	–	X	X	Same materials at peripheral and final seal faces, and same method of making seals (table A.7)	
5	–	–	X	X	Same basic substrate material (table A.2)	1)
6	–	–	X	X	Same external lead material, plating/coating process and material(s), and thickness of plating/coating (table A.7)	2)
NOTES 1 Applicable only when the substrate is an integral part of the sealing envelope (integral substrate package). 2 Only applicable where leads form part of the seal.						
Applicable test table: *Group 1* *Sub-group C2*	– vibration, swept frequency or – shock, followed by – acceleration, steady state					
1	X	X	X	X	Same or less severe test schedules and/or conditions	
2	–	X	X	X	Same package style/material and construction method (table A.7)	
3	X	X	X	X	Similarity within table A.8	
4	–	X	X	X	Same material(s), methods and process conditions used for encapsulation of the circuit (table A.7)	

Table A.10 *(continued)*

No.	Unencapsulated	Embedded	Cavity (organic seal)	Cavity (inorganic seal)	Criteria	Notes
5	X	X	X	X	Same material specifications and process methods for attachment and connection of added components to substrate and substrate to package (tables A.3, A.4, A.5, A.6)	
6	–	X	X		Same materials at peripheral and final seal faces and same method of making seals (table A.7)	
7	–	X	X	X	Same lead cross-sectional dimensions at exit from package or seal (table A.7)	
8	X	–	–	–	Same lead cross-sectional dimensions at point of mounting	
9	–	X	X	X	Same or greater lead length along minimum seal path (table A.7)	1)
10	–	X	X	X	Same method of external lead anchorage direct to substrate – if applicable (table A.7)	
11	–	X	–	–	Same basic materials and methods for connection from lead-throughs inside package to internal circuitry (table A.4)	
12	X	X	X	X	Same external lead material, plating/coating process and substrate thickness within 10 % of nominal CQC (table A.2)	
13	X	X	–	–	Same basic substrate material (table A.2)	
14	X	X	–	–	Nominal substrate thickness within ±10 % of nominal CQC (table A.2)	
15	–	X	X	X	Same or lesser range of material(s) and same methods used for intra-connection links on or between substrates (table A.3)	
16	–	–	X	X	Same or less severe deflection of package base and lid under maximum specified acceleration (mathematical model acceptable) (table A.7)	
17	X	–	X	X	P_1 is the same or less, where: $P_1 = \frac{\text{weight of substrate assembly or component}}{\text{minimum specified cross section of attachment joint(s)}}$	2)
18	X	–	X	X	Same design rules relating to intra-connection (wire or tape), unsupported lengths and clearances	
19	X	X	X	X	Mass and dimensions within the limits of table A.9	1)
20	X	X	X	X	Same package mounting method used for tests	
21	X	X	X	X	Same lead hardness specifications (table A.7)	1)
22	–	–	X	X	Same filling, if non gaseous (table A.6)	
23	X	X	X	X	Same or lesser range of added passive component generic type (table A.6)	
24	X	X	X	X	Same or lesser range of added semiconductor component generic type (table A.5)	
25	X	X	X	X	Same or lesser range of basic film materials (table A.3)	

NOTES

1 Applicable only to circuits intended to be mounted by the leads.

2 Applicable to assembled substrate including any added components attached to cavity package base and also to individual added components attached to substrate.

Table A.10 *(continued)*

No.	Unencap-sulated	Embedded	Cavity (organic seal)	Cavity (inorganic seal)	Criteria	Notes
Applicable test table: *Group 2* *Sub-group C3*	– resistance to soldering heat – resistance to solvents – change of temperature – damp heat, steady state					
1	X	X	X	X	Same or less severe test schedule and/or conditions	
2	–	X	X	X	Same package style/material and construction method (table A.7)	
3	–	X	X	X	Similarity within table A.8	
4	–	X	X	X	Same material(s), methods and process conditions used for encapsulation of the circuit (table A.7)	
5	X	X	X	X	Same material specification(s) and process methods for attachment and connection of added components to substrate and substrate to package (table A.7)	
6	–	–	X	X	Same materials at peripheral and final seal faces and same method of making seals (table A.7)	
7	–	X	X	X	Same lead cross-sectional dimensions at exit from package or seal (table A.7)	
8	X	X	X	X	Same or greater basic lead spacing within any row of leads (table A.7)	
9	X	X	X	X	Same method of external lead anchorage direct to substrate – if applicable (table A.7)	
10	–	X	–	–	Same basic materials and methods for connection from lead-throughs inside package to internal circuitry (table A.7)	
11	X	X	X	X	Same external lead material, plating/coating process and material(s) and thickness of plating/coating (table A.7)	
12	X	X	X	X	Same basic substrate material (table A.2)	
13	–	X	–	–	Nominal substrate thickness within ±10 % of nominal CQC (table A.2)	1)
14	–	X	X	X	Same or greater insulation surface distance at exit of lead(s) from seal (table A.7)	
15	–	X	X	X	Same or lower mean voltage gradient across the insulation surface at exit of lead(s) from seal, as identified from rated electrical conditions (table A.7)	
16	–	X	–	–	Same or greater thickness of embedding plastic(s) over critical interfaces (table A.7)	
17	X	X	X	X	Same marking material system and method of application (table A.7)	
18	–	X	X	X	Same or greater lead length along minimum seal path (table A.7)	
19	X	X	X	X	Same or lesser range of basic film materials (table A.3)	

NOTE 1 – These requirements can be collectively waived by demonstrating that the circuit structure is such that, compared to the CQC, the same or lower temperature rise at comparable material interfaces occurs during the solder heat test.

Table A.10 *(continued)*

No.	Unencap-sulated	Embedded	Cavity (organic seal)	Cavity (inorganic seal)	Criteria	Notes
20	X	X	X	X	Same basic film process (tableau A.3)	
21	-	X	-	-	Same design rules relating intra-connections (wire or tape), free lengths and clearances (tables A.4, A.6)	
22	X	X	X	X	Same or lesser range of added passive component generic types (table A.6)	
23	X	X	X	X	Same or lesser range of added semiconductor component generic types (table A.4)	

Applicable test table: – solderability
Group 3 – tensile
Sub-group D2 – bending
– thrust

1	-	X	X	X	Same package style/material and construction method (table A.7)	
2	-	X	X	X	Similarity within table A.8	1)
3	-	X	X	X	Same material(s), methods and process conditions used for encapsulation of the circuit (table A.7)	
4	-	X	X	X	Same lead cross-sectional dimensions at exit from package or seal (table A.7)	
5	-	X	X	X	Same lead hardness specification (table A.7)	
6	-	X	X	X	Same or greater basic lead spacing within any row of leads (table A.7)	1)
7	X	X	X	X	Same basic external lead material, plating/coating process and material(s) (table A.7)	
8	-	X	X	X	Same method of external lead anchorage direct to substrate, if applicable (table A.7)	
9	-	X	X	X	Same or greater lead length along minimum seal path (table A.7)	2)
10	-	-	X	X	Same insulation (basic) material used for lead seals (table A.7)	
11	-	X	X	X	Same or greater minimum external cross-sectional area of individual leads (table A.7)	3)
12	-	X	X	X	Same or less meniscus height permitted on leads at exit from seal surface plane	
13	X	X	X	X	Same solderability assessment method and equipment used	

NOTES

1 Applicable to bending (row) only.

2 Applicable only to cavity packages with metal bodies.

3 Applicable to tensile and bending (wire/strip) only.

Tableau A.10 *(continued)*

No.	Unencap-sulated	Embedded	Cavity (organic seal)	Cavity (inorganic seal)	Criteria	Notes
Applicable test table: *Group 4* *Sub-group C4*	– cold storage – dry heat storage					
1	X	X	X	X	Same or less severe test schedules and/or conditions	
2	–	X	X	X	Same package style/material and construction method (table A.7)	
3	X	X	X	X	Similarity within table A.8	
4	–	X	–	–	Same material(s), methods and process conditions used for encapsulation of the circuit (table A.7)	
5	X	X	X	X	Same material specification(s) and process methods for attachment and connection of added components to substrate and substrate to package (tables A.4 to A.7)	
6	–	–	X	X	Same materials at peripheral and final seal faces and same method of making seals (table A.7)	
7	–	–	X	X	Same internal gas or other filling, including any impurity and water content specifications (table A.7)	
8	X	X	X	X	Same basic substrate material (table A.2)	
9	X	X	X	X	Same or lesser range of added passive component generic types (table A.6)	
10	X	X	X	X	Same or lesser range of added semiconductor component generic types (tables A.4 and A.5)	
11	X	X	X	X	Comparable requirements in the stability of film and added circuit elements (dry heat only) (tables A.2 to A.6)	
12	X	X	X	X	Same or lesser range of basic film materials (table A.3)	
13	X	X	X	X	Same basic film process (table A.3)	

Tableau A.10 *(continued)*

No.	Unencap-sulated	Embedded	Cavity (organic seal)	Cavity (inorganic seal)	Criteria	Notes
Applicable test table: *Group 5* *Sub-group D1*	– endurance 1 000 h – endurance 2 000 h					
1	X	X	X	X	Same or less severe test schedule(s) and/or conditions	
2	–	X	X	X	Same package style/material and construction method (table A.6)	
3	–	X	X	X	Similarity within table A.8	
4	–	X	X	–	Same material(s), methods and process conditions used for encapsulation of the circuit (table A.7)	
5	X	X	X	X	Same material specification(s) and process methods for attachment and connection of added components to substrate and substrate to package (tables A.4 to A.7)	
6	–	–	X	X	Same materials at peripheral and final seal faces and same method of making seals (table A.7)	
7	–	–	X	X	Same internal gas or other filling, including any impurity and water content specifications (table A.7)	
8	X	X	X	X	Same basic substrate material (table A.2)	
9	X	X	X	X	Same or lesser range of added passive component generic types (table A.6)	
10	X	X	X	X	Same or lesser range of added semiconductor component generic types (tables A.4 and A.5)	
11	X	X	X	X	Same or lower maximum temperature at comparable material interfaces under rated electrical conditions of use	
12	X	X	X	X	Comparable or lesser requirements in the stability of the film and added circuit elements (tables A.3 to A.5)	
13	X	X	X	X	Same or lesser range of basic film materials (table A.3)	
14	X	X	X	X	Same basic film process (table A.3)	
15	X	X	X	X	Same geometrical, electrical and thermal design rules applied to film layout (table A.3)	
16	X	X	X	X	Same trimming process applied to film elements (table A.3)	

Appendix B

Minimum contents of a manufacturer's capability manual for thick film circuits

B.1 Scope

This appendix establishes the requirements for the capability manual for thick film and hybrid thick film integrated circuits. It does not apply to thin film or semiconductor integrated circuits.

The term hybrid is defined in 2.4.13 of the generic specification and the scope of this appendix includes the use of any of the added components in association with the basic thick film technology.

NOTE - In addition to the requirements stated herein the manufacturer may include additional information, e.g. on process control and inspection schedules, which he considers necessary for the full control of his capability.

For ease of reference the capability manual shall give information under the headings given below as appropriate. Under item 1 of the capability manual, the manufacturer shall declare the entire scope of his capability and state which assessment level applies. Where the procedure under 3.2 of the generic specification is invoked, the capability manual shall make reference to the surveillance of those stages which are not carried out under the direct surveillance of an approval chief inspector.

B.2 Customer participation in the layout

The manufacturer shall declare whether he permits customer participation in the technological design and layout of circuits. In the case of a device manufactured to this standard where the customer has provided the design and layout, it shall be the responsibility of the manufacturer to ensure that his approved design and layout rules have been followed.

B.3 Capability abstract

The statement of basic technology in addition to the details required in table 1 of the generic specification for film and hybrid film integrated circuits shall include the following which shall be used in the QPL:

a) type of substrate, e.g. alumina, beryllium oxide;

b) types of inks, numbers of layers and methods of pattern formation, e.g. screen printing, ink writing;

c) range of film elements, e.g. conductors, resistors, capacitors, etc.;

d) methods of trimming of film elements, e.g. laser, spark erosion, air abrasion;

e) methods of lead attachment to the substrate, e.g. soldering;

f) basic encapsulation method, e.g. hermetic, plastic;

g) types of added components, e.g. chip capacitors, discrete semiconductor devices, semiconductor dice and related methods of attachment;

h) methods of interconnecting within the circuits according to type, e.g. bonding, soldering;

i) (not for integral substrate packages) Methods of attaching substrate to package, e.g. eutectic bond, organic bond, etc.;

j) boundaries of capability – range of values/tolerance, matching where appropriate, conductors, resistors, capacitors, etc.

NOTE - It may not be possible to achieve all the limits of the capability in combination.

B.4 Materials and added components

This section of the capability manual shall:

a) identify and provide evidence of the existence of purchasing specifications for the materials which are critical for the quality of the circuits;

b) describe the methods used to verify the suitability of materials for production and identify the documentation necessary to ensure consistent quality of the specified materials;

c) indicate the inspection methods for added components (see 3.6.2 of the generic specification).

B.4.1 *Material purchasing specifications*

The manual shall identify the relevant purchasing specifications under the appropriate headings as listed below. The "Specification contents" column lists the data which shall be included in the purchasing specifications but such data is not required in the capability manual. The list of items included in each subclause is intended for guidance and is not exhaustive. Items are applicable where relevant to the particular process technology.

B.4.1.1 *Materials in circuit and package*

	Specification contents
B.4.1.1.1 Substrates	Types of materials, composition and characteristics, thermal and mechanical characteristics
B.4.1.1.2 Printing inks, pastes and glazes	Types, composition and characteristics
B.4.1.1.3 Assembly materials	Types of materials, e.g. lead frames, adhesives, solders, leads and terminations, varnishes

	Specification contents (continued)
B.4.1.1.4 Added components	Types, specification numbers or other reference data of the added components approved for use. Information on preferred types of components. In addition, the capability manual shall provide details of an appropriate purchasing system, and inspection and testing requirements for added components
B.4.1.1.5 Package and encapsulation materials	Types of materials, e.g. cases, caps, lids, finishes, platings, mouldings, thermosetting resins, varnishes, coatings, identification and marking Material combinations, e.g. Kovar-glass, glass-ceramic Type of plastic used for plastic or part plastic encapsulations List of standard packages used, or reference to control of drawings for non-standard packages
B.4.1.2 *Materials used in processing*	
B.4.1.2.1 Artwork	Types and characteristics of materials used in circuit design and artwork, e.g. dimensional stability, durability
B.4.1.2.2 Printing screens	Types, mesh characteristics
B.4.1.2.3 Processing materials	Types of materials, chemicals used in circuit preparation, adjustment, trimming
B.4.1.2.4 Assembly materials	Types and characteristics of materials used as aids to assembly, e.g. cleaning agents

B.4.2 *Material verification*

The manual shall describe any method for the verification of the suitability of the above materials for production and any other documentation necessary to ensure the consistent quality of those materials which are critical to the quality of the circuits.

B.5 Design data and layout rules

Reference shall be made to the detailed rules in the design and layout of circuits. The manual shall contain the following data as appropriate.

Characteristics	*Design limit(s) to be stated*	
a) *Conductor tracks*		
Track width	Min.	
Track thickness	Min.	Max.
Spacing between parallel tracks	Min.	
Spacing between track, bonding pad, terminal pad or nay combination thereof	Min.	
Spacing between any metallization and edge of substrate	Min.	
Terminal pad dimensions	Min.	
Probe pad dimensions	Min.	
Conductor track resistivity		Max.
Current density for each conductor material		Max.
Track dissipation		Max.
Any requirements for solder build up of tracks		
Solderability characteristics by brazing		
Bondability characteristics		
Voltage stress which can be applied between parallel tracks at minimum design spacing		Max.
Insulation resistance under same conditions	Min.	
Dimensions of lead-through holes Spacing of lead-through holes from edge of substrate	Min.	
Track adhesion after processing/ageing	Min.	
Mounting pad geometry, dimensions, positional tolerances for each type of added component, spacing from other tracks		
Wire-bonding or other interconnecting pad dimensions	Min.	
Spacing between tracks under chip capacitors	Min.	
Rules relating to underpassing conductors		

Characteristics	*Design limit(s) to be stated*	
b) *Dielectric and cross-over insulation, capacitance*		
Overlap of dielectric over conductor track	Min.	
Thickness of dielectric	Min.	
Capacitance of cross-over (per unit area)		Max.
Spacing of dielectric to edge of substrate	Min.	
Insulation resistance of dielectric (per unit area)	Min.	
Range of capacitance values	Min.	Max.
Voltage breakdown	Min.	
c) *Resistors*		
Range of resistor values	Min.	Max.
Temperature coefficient of resistance		Max.
Dissipation per unit area of stated surface at ambient temperature		Max.
Stability % per 1 000 h at maximum dissipation		Max.
Stability % per 1 000 h at maximum voltage stress		Max.
Noise data – where low noise performance is claimed		Max.
Non-linearity (IEC Publication 440)		Max.
For rectangular resistors		
Linear dimensions	Min.	Max.
Aspect ratio (length/width)	Min.	Max.
For other resistor profiles		
Design rules with limits as necessary		
For all resistors		
Overlap of resistor on conductor track	Min.	
Undisturbed conductor track width (for single resistor)	Min.	
Distance of probe pad from end of resistor		Max.
Spacing from resistor to conductor track	Min.	
Spacing between resistor material	Min.	
Glaze or protection overlap	Min.	

Characteristics	*Design limit(s) to be stated*
c) *Resistors* (continued)	
For each type of trimming	
Rules for trimming including limiting conditions	
Tolerance relating to size and ohmic value after trimming as appropriate	Min.
Matching tolerance after trimming	Min.
Tracking tolerance after trimming	Min.

Where appropriate, additional data shall be given on:

the effect of resistivity of terminal materials particularly for short profile resistors;

high voltage stability;

noise and design requirements for low-noise resistors.

Where the realization of the circuit pattern is by means other than screen printing many of the above requirements shall apply and shall be given as appropriate.

d) *Glass and protection*

Where appropriate, the requirements for glaze and other protection for circuit elements shall be stated.

e) *Solder and braze*

Where appropriate, the requirements for solder and braze compositions used either by overprinting or by syringe application shall be declared.

f) *Pattern registration*

Data on the dimensional tolerances for pattern registration.

g) *Added components*

Positional tolerances relating component tab, wire or other termination to the area of mounting pad	Min.
Distance between adjacent added components	Min.
Distance between edges of added components and adjacent film areas	Min.
Distance between edge of component and edge of substrate	Min.
Clearance between assembled circuit, including added components and inside of package	Min.

Characteristics — *Design limit(s) to be stated*

h) *(Not for integral substrate packages)*

The basic methods used for attachment of substrates to packages shall be stated (e.g. eutectic bond, organic bond, etc.).

Maximum values for the dimensions and mass of the substrate assembly carried by the attachment shall be related to limiting conditions for thermal shock, mechanical shock, vibration, acceleration, thermal resistance and (for non cavity packages only) humidity.

i) *Thermal characteristics*

Thermal resistance or power dissipation of substrate/package combinations	Max.
Temperature and temperature gradients	Max.
Rules or data relating density and spacing of power dissipating elements such as resistors and rectifiers	
Rules or data relating density and spacing of power dissipating circuit elements such as semiconductor devices with respect to the thermal characteristics of substrate and package combinations	
Means of establishing that the maximum ratings of a component, e.g. temperature, are not being exceeded in the substrate/package environment	

B.6 Flow charts

The manual shall include one or more detailed flow charts showing all stages of manufacture and identifying the procurement specifications, process specifications, inspection and quality control checks by reference to in-house documentation.

The flow charts shall show full sequence of events and shall include the following activities:

a) *Design verification*

Method checking that the circuit design and layout are in conformity with the design data, layout rules and circuit requirements. The requirements for pre-production design verification trials shall also be referenced

b) *Masks*

Procedures for the identification, control and replacement of masks

c) *Ink blending*

Procedures for the issue, blending and checking of inks

d) *Printing and firing*

Issue, preparation and inspection of substrates prior to printing
Method of ensuring accurate registration of masks and substrates
Printing of each ink pattern
Requirements for drying and pre-firing inspection
Requirements for control of firing schedules
Requirements for glass or other protection
Post firing inspection

e) *Resistor trimming*

Trimming procedures and method of ensuring conformance with design rules e.g. dimensional limitations in trimmed region, trimming to function, trimming by isolation

f) *Lead attachment*

Issue, preparation and inspection of lead frames, terminations and other piece parts a appropriate
Requirements for the attachment of leads to substrates
Requirements for pre-assembly inspection

g) *Assembly*

Requirements for initial substrate protection, e.g. varnish

Issue, inspection, preparation, pre-forming and sub-assembly of added component prior to, during or after assembly on the fired substrate

1) *For film integrated circuits or elements*

   External visual inspection
   Electrical inspection in accordance with relevant detail specification
   Requirements for attachment and interconnection

2) *For discrete capacitors and resistors*

   External visual and electrical inspection in accordance with specified measurements as appropriate
   Requirements for lead forming
   Requirements for attachment and interconnection

3) *For chip capacitors and resistors*

   External visual and electrical inspection in accordance with relevant detail specification
   Requirements for attachment and interconnection

4) *For discrete semiconductor devices*

   External visual inspection as appropriate
   Electrical inspection in accordance with relevant detail specification
   Requirements for lead forming
   Requirements for attachment and interconnection

5) *For unencapsulated semiconductor dice*

Pre-assembly inspection in accordance with specified requirements

Requirements for carrier or sub-assembly mounting as appropriate

Electrical inspection in accordance with relevant detail specification

Attachment to substrate

Wire material and attachment process

6) *For all types of added components*

Requirements for post-assembly inspection of the assembled substrate prior to encapsulation

When appropriate, requirements for post-assembly circuit trimming

Rework instructions regarding the conditions under which added components may be reclaimed, inspected and re-used, and/or the conditions under which substrates may be reclaimed, inspected and re-used after the removal of suspect or faulty added components and the maximum number of rework cycles in each case

h) *Final sealing*

Requirements for pre-encapsulation inspection

Issue, preparation and inspection of encapsulation materials, preforms, bases, caps, lids, epoxies, prior to use

Sealing process

Post-encapsulation inspection

Marking and lead identification

i) *Final test*

Requirements for the acceptance testing of completed circuits

Final inspection and packing for dispatch

j) *Rework*

Additionally the charts shall show where rework may take place and identify the controlling specifications. These specifications shall conform to the applicable requirements and shall state the maximum number of rework cycles in each case

B.7 Capability qualifying circuits

To satisfy the requirements, the manual shall detail the CQCs to be used for assessment and shall indicate for each circuit the aspect or aspects of the declared capability which are being assessed.

Every CQC shall have a detail specification which includes a dimensioned layout drawing. Specifications for packaged CQCs shall be in the style and content of the relevant blank detail specification.

NOTE - A group of CQCs may be included in a single specification.

The range of CQCs used shall, as a minimum, assess the following characteristics of the capability, as appropriate.

B.7.1 *Limits and rules for circuit design and processing*

a) *Conductor characteristics* (film)

i) Conductor resistivity for all basic conductor materials

ii) Insulation resistance between tracks at minimum design spacing for each basic material type

iii) Breakdown voltage between tracks at minimum design spacing for each basic material type

iv) Maximum current carrying capacity for each basic material type

v) Capacitance of crossovers

vi) Breakdown voltage of crossovers

vii) Maximum number of conductor layers for each basic material type

viii) Insulation resistance between conductors at minimum design spacing for each basic material type for each conductor layer

ix) Insulation resistance between adjacent conductor layers

x) Insulation resistance between underpassing conductor and added component termination at minimum design spacing

xi) Minimum size of the vias

xii) Insulation resistance between trimmed resistor termination and underpassing conductor

b) *Resistor characteristics* (film)

i) Minimum, maximum and intermediate resistance values for each resistor ink series terminated by each basic conductor material type

ii) Trimmed resistor tolerance for each ink series for laser and/or abrasive methods

iii) Resistor matching for each ink series

iv) Temperature coefficient of resistance (absolute and tracking) for each ink series

v) Minimum and maximum aspect ratios for each resistor ink series

vi) Smallest physical size for each resistor ink series

vii) All preceding resistance characteristics with respect to each resistance ink series screened on printed dielectric layers

c) *Capacitor characteristics* (film)

i) Minimum, maximum and intermediate capacitance values

ii) Capacitance tolerance

iii) Dissipation factor

iv) Temperature coefficient of capacitance

v) Capacitance tracking with temperature

d) *Added components*

  i) All attachment methods
  ii) Maximum mass to contact area ratio for each added component type
  iii) All interconnection methods
  iv) Maximum differential expansion strain

B.7.2 *Packaging*

a) *Solid encapsulated and unencapsulated circuits*

Packages having the maximum number of lead-out positions for each basic package type

b) *Cavity packages*

Packages having the maximum number of lead-out positions and/or greatest seal length with the same sealing method for each basic package type

B.7.3 *Endurance characteristics*

Circuits designed to the maximum declared design rule combinations of power dissipation and operating temperature shall be assessed for each basic package type.

B.7.4 *Post-test end points*

All major static and dynamic tests, with extended limits where necessary, shall be included in the post end points except resistor matching.

Appendix C

Minimum contents of a manufacturer's capability manual for thin film circuits

C.1 Scope

This appendix establishes the requirements for the capability manual for thin film and hybrid thin film integrated circuits. It does not apply to thick film or semiconductor integrated circuits.

The term hybrid is defined in 2.4.13 of the generic specification and the scope of this appendix includes the use of any of the added components in association with the basic thin film technology.

NOTE - In addition to the requirements stated herein the manufacturer may include additional information, e.g. on process control and inspection schedules, which he considers necessary for the full control of his capability.

For ease of reference, the capability manual shall give information under the headings given below as appropriate. Under item 1 of the capability manual, the manufacturer shall declare the entire scope of his capability and state which assessment level applies. Where the procedure under 3.2 of the generic specification is invoked, the capability manual shall make reference to the surveillance of those stages which are not carried out under the direct surveillance of an approved chief inspector.

C.2 Customer participation in the layout

The manufacturer shall declare whether he permits customer participation in the technological design and layout of circuits. In the case of a device manufactured to this standard where the customer has provided the design and layout, it shall be the responsibility of the manufacturer to ensure that his approved design and layout rules have been followed.

C.3 Capability abstract

The statement of basic technology in addition to the details required in table 1 of the generic specification for film and hybrid film integrated circuits shall include the following which shall be used in the QPL:

a) type of substrate, e.g. glass, glazed ceramic, as-fired ceramic;
b) method of film deposition, e.g. vacuum evaporation, sputtering;
c) method of pattern formation, e.g. photolithography, spark erosion, microengraving;

d) range of film elements, e.g. conductors, resistors, capacitors, etc.;

e) methods of trimming of film elements, e.g. laser, spark erosion, air abrasion;

f) methods of lead attachment to the substrate, e.g. soldering;

g) basic encapsulation method, e.g. hermetic, plastic;

h) types of added components, e.g. chip capacitors, discrete semiconductor devices, semiconductor dice and related methods of attachment;

i) methods of interconnecting within the circuits according to type, e.g. bonding, soldering;

j) (not for integral substrate packages) Methods of attaching substrate to package, e.g. eutectic bond, organic bond, etc.;

k) boundaries of capability – range of values/tolerance, matching where appropriate, conductors, resistors, capacitors, etc.

NOTE - It may not be possible to achieve all the limits of the capability in combination.

C.4 Materials and added components

This section of the capability manual shall:

a) identify and provide evidence of the existence of purchasing specifications for the materials which are critical for the quality of the circuits;

b) describe the methods used to verify the suitability of materials for production and identify the documentation necessary to ensure consistent quality of the specified materials;

c) indicate the inspection methods for added components (see 3.6.2 of the generic specification).

C.4.1 *Material purchasing specification*

The manual shall identify the relevant purchasing specifications under the appropriate headings as listed below. The "Specification contents" column lists the data which shall be included in the purchasing specifications but such data is not required in the capability manual. The list of items included in each subclause is intended for guidance and is not exhaustive. Items are applicable where relevant to the particular process technology.

C.4.1.1 *Materials in circuit and package*

	Specification contents
C.4.1.1.1 Substrates	Types of materials, composition and characteristics, thermal and mechanical characteristics
C.4.1.1.2 Deposited materials	Types, composition and characteristics
C.4.1.1.3 Assembly materials	Types of materials, e.g. lead frames, adhesives, solders, leads and terminations, varnishes

	Specification contents (continued)
C.4.1.1.4 Added components	Types, specification numbers or other reference data of the added components approved for use. Information on preferred types of components. In addition, the capability manual shall provide details of an appropriate purchasing system, and inspection and testing requirements for added components
C.4.1.1.5 Package and encapsulation materials	Types of materials, e.g. cases, caps, lids, finishes, platings, mouldings, thermosetting resins, varnishes, coatings, identification and marking Material combinations, e.g. Kovar-glass, glass-ceramic Type of plastic used for plastic or part plastic encapsulations List of standard packages used, or reference to control of drawings for non-standard packages
C.4.1.2 *Materials used in processing*	
C.4.1.2.1 Artwork	Types and characteristics of materials used in circuit design and artwork, e.g. dimensional stability, durability.
C.4.1.2.2 Printing screens	Types and characteristics of photographic plates, emulsions, masks, electrodes, etchants
C.4.1.2.3 Processing materials	Types of materials, chemicals used in circuit preparation, trimming, adjustment
C.4.1.2.4 Assembly materials	Types and characteristics of materials used as aids to assembly, e.g. cleaning agents

C.4.2 *Material verification*

The manual shall describe any method for the verification of the suitability of the above materials for production and any other documentation necessary to ensure the consistent quality of those materials which are critical to the quality of the circuits.

C.5 Design data and layout rules

Reference shall be made to the detailed rules in the design and layout of circuits. The manual shall contain the following data as appropriate.

Characteristics	*Design limit(s) to be stated*	
a) *Conductor tracks*		
Track width	Min.	
Track thickness	Min.	Max.
Spacing between parallel tracks	Min.	
Spacing between track, bonding pad, terminal pad or any combination thereof	Min.	
Spacing between any metallization and edge of substrate	Min.	
Terminal pad dimensions	Min.	
Probe pad dimensions	Min.	
Conductor track resistivity		Max.
Current density for each conductor material		Max.
Track dissipation		Max.
Any requirements for solder build up of tracks		
Solderability characteristics by brazing		
Bondability characteristics		
Voltage stress which can be applied between parallel tracks at minimum design spacing		Max.
Insulation resistance under same conditions	Min.	
Dimensions of lead-through holes		
Spacing of lead-through holes from edge of substrate	Min.	
Track adhesion after processing/ageing	Min.	
Mounting pad geometry, dimensions, positional tolerances for each type of added component, spacing from other tracks		
Wire-bonding or other interconnecting pad dimensions	Min.	
Spacing between tracks under chip capacitors	Min.	
Rules relating to underpassing conductors		

Characteristics	*Design limit(s) to be stated*	
b) *Dielectric and cross-over insulation, capacitance*		
Overlap of dielectric over conductor track	Min.	
Thickness of dielectric	Min.	
Capacitance of cross-over (per unit area)		Max.
Spacing of dielectric to edge of substrate	Min.	
Insulation resistance of dielectric (per unit area)	Min.	
Range of capacitance values	Min.	Max.
Voltage breakdown	Min.	
c) *Capacitors*		
Range of capacitance values	Min.	Max
Capacitance per unit area	Min.	Max.
Insulation resistance, for example per unit area	Min.	
Voltage breakdown, operating voltage, Tan δ, Q	Min.	Max. (as appropriate)
Capacitance stability under conditions	Min.	
Temperature coefficient (TCC) over stated range		
Matching tolerance after trimming		
d) *Resistors*		
For untrimmed resistors		
Range of resistor values	Min.	Max.
Temperature coefficient of resistance		Max.
Dissipation per unit area of stated surface at ambient temperature		Max.
Stability % per 1 000 h at maximum dissipation		Max.
Stability % per 1 000 h at maximum voltage stress		Max.
For rectangular resistors		
Linear dimensions	Min.	Max.
Aspect ratio (length/width)	Min.	Max.
For other resistor profiles		
Design rules with limits as necessary		

Characteristics	*Design limit(s) to be stated*	
d) *Resistors* (continued)		
For all resistors		
Overlap of resistor on conductor track	Min.	
Undisturbed conductor track width (for single resistor)	Min.	
Distance of probe pad from end of resistor		Max.
Spacing from resistor to conductor track	Min.	
Spacing between resistor material	Min.	
Glaze or protection overlap	Min.	
For trimming resistors		
Rules for trimming including limiting conditions		
Tolerance relating to size and ohmic value after trimming as appropriate	Min.	
Matching tolerance after trimming	Min.	
Tracking tolerance after trimming	Min.	
Where appropriate, additional data shall be given on:		
the effect of resistivity of terminal materials particularly for short profile resistors;		
high voltage stability;		
noise and design requirements for low-noise resistors;		
non-linearity (IEC Publication 440)		Max.

e) *Glass and protection*

Where appropriate, the requirements for glass and other protection for circuit elements shall be stated.

f) *Solder and conducting organic materials*

Where appropriate, the requirements for solder and other conducting compositions used either by solder dipping, printing or by dispenser (for example syringe) application shall be declared.

g) *Pattern registration*

Data on the dimensional tolerances for pattern registration.

Characteristics	*Design limit(s) to be stated*
h) *Added components*	
Positional tolerances relating component tab, wire or other termination to the area of mounting pad	Min.
Distance between adjacent added components	Min.
Distance between edges of added components and adjacent film areas	Min.
Distance between edges of component and edge of substrate	Min.
Clearance between assembled circuit, including added components and inside of package	Min.
Requirements for mounting semiconductor dice on carriers or subassemblies	

i) *(Not for integral substrate packages)*

The basic methods used for attachment of substrates to packages shall be stated (e.g. eutectic bond, organic bond, etc.).

Maximum values for the dimensions and mass of the substrate assembly carried by the attachment shall be related to limiting conditions for thermal shock, mechanical shock, vibration, acceleration, thermal resistance and (for non cavity packages only) humidity.

j) *Thermal characteristics*	
Thermal resistance or power dissipation of substrate/package combinations	Max.
Temperature and temperature gradients	Max.
Rules or data relating density and spacing of power dissipating elements such as resistors and rectifiers	
Rules or data relating density and spacing of power dissipating circuit elements such as semiconductor devices with respect to the thermal characteristics of substrate and package combinations	
Means of establishing that the maximum ratings of a component, e.g. temperature, are not being exceeded in the substrate/package environment	

C.6 Flow charts

The manual shall include one or more detailed flow charts showing all stages of manufacture and identifying the procurement specifications, process specifications, inspection and quality control checks by reference to in-house documentation.

The flow charts shall show the full sequence of events and shall include the following activities:

a) *Design verification*

Method of checking that the circuit design and layout are in conformity with the design data, layout rules and circuit requirements. The requirements for pre-production design verification trials shall also be referenced

b) *Masks*

Procedures for the identification, control and renewal of photographic masks, metal masks

c) *Deposited materials*

Procedures for control of material issue and validation of composition prior to and during use

d) *Deposition*

Storing and release, preparation (including cleaning) and inspection of substrates prior to film deposition
Method of ensuring accurate registration of screens and substrates
Deposition of each successive material/layer
Requirements for control of deposition processes
Requirements for stabilization by heat treatment
Requirements for glaze or other protection
Post deposition inspection

e) *Trimming*

Trimming procedures and method of ensuring conformance with design rules, e.g. dimensional limitations in trimmed region, trimming to function, trimming by isolation

f) *Lead attachment*

Storing and release, preparation and inspection of lead frames, terminations and other piece parts as appropriate
Requirements for pre-assembly inspection
Attachment of leads to substrates

g) *Assembly*

Requirements for initial substrate protection, e.g. varnish

Issue, inspection, preparation, pre-forming and sub-assembly of added components prior to, during, or after assembly on the fired substrate

1) *For film integrated circuits or elements*

   External visual inspection
   Electrical inspection in accordance with relevant detail specification
   Requirements for attachment and interconnection

2) *For discrete encapsulated capacitors and resistors*

   External visual and electrical inspection in accordance with specified measurements as appropriate
   Requirements for lead forming
   Requirements for attachment and interconnection

3) *For chip capacitors and resistors*

   External visual and electrical inspection in accordance with relevant detail specification
   Requirements for attachment and interconnection

4) *For discrete encapsulated semiconductor devices*

   External visual inspection as appropriate
   Electrical inspection in accordance with relevant detail specification
   Requirements for lead forming
   Requirements for attachment and interconnection

5) *For unencapsulated semiconductor dice*

   Pre-assembly inspection in accordance with specified requirements
   Requirements for carrier or sub-assembly mounting as appropriate
   Electrical inspection in accordance with relevant detail specification
   Attachment to substrate
   Wire material and attachment process

6) *For all types of added components*

   Requirements for post-assembly inspection of the assembled substrate prior to encapsulation
   When appropriate, requirements for post-assembly circuit trimming
   Rework instructions regarding the conditions under which added components may be reclaimed, inspected and re-used, and/or the conditions under which substrates may be reclaimed, inspected and re-used after the removal of suspect or faulty added components and the maximum number of rework cycles in each case

h) *Final sealing*

Requirements for pre-encapsulation inspection

Issue, preparation and inspection of encapsulation materials, preforms, bases, caps, lids, epoxies, prior to use

Sealing process

Post-encapsulation inspection

Marking and lead identification

i) *Final test*

Requirements for the acceptance testing of completed circuits

Final inspection and packing for dispatch

j) *Rework*

Additionally the charts shall show where rework may take place and identify the controlling specifications. These specifications shall conform to the applicable requirements and shall state the maximum number of rework cycles in each case.

C.7 Capability qualifying circuits

To satisfy the requirements, the manual shall detail the CQCs to be used for assessment and shall indicate for each circuit the aspect or aspects of the declared capability which are being assessed.

Every CQC shall have a detail specification which includes a dimensioned layout drawing. Specifications for packaged CQCs shall be in the style and content of the relevant blank detail specification.

NOTE - A group of CQCs may be included in a single specification.

The range of CQCs used shall, as a minimum, assess the following characteristics of the capability, as appropriate.

C.7.1 *Limits and rules for circuit design and processing*

a) *Conductor characteristics* (film)

- i) Conductor resistivity for all basic conductor materials.
- ii) Insulation resistance between tracks at minimum design spacing for each basic material type.
- iii) Breakdown voltage between tracks at minimum design spacing for each basic material type.
- iv) Current carrying capacity for each basic material type.
- v) Capacitance of crossovers.
- vi) Breakdown voltage of crossovers.
- vii) Maximum number of conductor layers for each basic material type.
- viii) Insulation resistance between conductors at minimum design spacing for each basic material type for each conductor layer.
- ix) Insulation resistance between adjacent conductor layers.
- x) Insulation resistance between underpassing conductor and added component termination at minimum design spacing.
- xi) Minimum size of the vias.
- xii) Insulation resistance between trimmed resistor termination and underpassing conductor.

b) *Resistor characteristics* (film)

- i) Minimum, maximum and intermediate resistance values for resistors terminated by each conductor material type.
- ii) Trimmed resistor tolerance for laser and/or abrasive methods.
- iii) Resistor matching for each ink series.
- iv) Temperature coefficient of resistance (absolute and tracking).
- v) Minimum and maximum aspect ratios.
- vi) Smallest physical size.
- vii) Non-rectangular resistor profiles.

c) *Capacitor characteristics* (film)

- i) Minimum, maximum and intermediate capacitance values.
- ii) Capacitance tolerance.
- iii) Dissipation factor.
- iv) Temperature coefficient of capacitance.
- v) Capacitance tracking with temperature.

d) *Added components*

- i) All attachment methods.
- ii) Maximum mass to contact area ratio for each added component type.
- iii) All interconnection methods.
- iv) Maximum differential expansion strain.

C.7.2 *Packaging*

a) *Solid encapsulated and unencapsulated circuits*

Packages having the maximum number of lead-out positions for each basic package type.

b) *Cavity packages*

Packages having the maximum number of lead-out positions and/or greatest seal length with the same sealing method for each basic package type.

C.7.3 *Endurance characteristics*

Circuits designed to the maximum declared design rule combinations of power dissipation and operating temperature shall be assessed for each basic package type.

C.7.4 *Post-test end points*

All major static and dynamic tests, with extended limits where necessary, shall be included in the post end points except resistor matching.